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A probability distribution analyser for TV signals

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A PROBABILITY DISTRIBUTION ANALYSER FOR TV SIGNALS

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SUMMARY

A new tool, a Probability distribution analyser has been developed and is described in this Report. The analyser measures the probability distribution function of digital video signals and displays this on an oscilloscope.

Experiments to compare the performance of two different predictors for use in a differential pulse code modulation coder have been performed using the analyser. It has also been used in conjunction with video noise reduction equipment to measure the noise power in a stationary picture.

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A PROBABILITY DISTRIBUTION ANALYSER FOR TV SIGNALS

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1. Introduction

This Report describes an analyser which measures and displays the probability distribution function (PDF) of a digital video signal. Its use will be illustrated by describing two applications in which it has been used to examine the PDF of signals which have been derived by digitally processing composite PAL signals. In each case it has been possible to examine the PDF with the object of either extracting particular information from the signal or of optimising the signal processing.

The usefulness of such an analyser is not confined to these particular examples, and it should prove to be a useful general purpose tool for gaining insight into the characteristics of digital television signals.

2. Principle of operation

The PDF of a digital signal can be determined by measuring the number of times each signal value occurs and storing this data. The measurement period must be suitably chosen so that sufficient data points are used to produce an accurate distribution and will depend intimately on the nature of the signal being measured. Often the distribution will be normalised by dividing each number of occurrences by the total number of measurements. In a practical system it is convenient to measure the absolute number of occurrences and it the number of samples measured is constant, the result does not have to be normalised. Although this requires a store with a large word length it is preferable to normalising because of the limited speed with which division can be performed in hardware.

3. Design considerations

The major applications for the analyser are in digital video. These applications lead to four important design considerations. They are:

A) What is the typical data rate of digital video signals?

Many projects use a clock frequency of 13.5 MHz and the analyser must be compatible with this. Further more the hardware design becomes increasingly more complicated as the clock frequency is raised. For these reasons it is designed with TTL logic to operate up to a maximum clock frequency of 13.5 MHz.

(B) What is the maximum measurement interval?

In a 625-line video signal the duration of an active television field (approximately 18.4 ms) is a suitable measurement interval because it ensures that sufficient data is accumulated to produce an accurate probability distribution. The combination of a 13.5 MHz sampling frequency and an 18.4 millisecond active field results in about 248,000 samples in each active field. At worst the same data value might occur for all the data samples. An 18 bit binary word would then be required to store the number of times it had occurred. In practice the probability of this happening is very small and it is convenient to restrict the word length to 16 bits.

(C) What is the maximum number of levels in the video signal?

Currently most digital T.V. systems use 8 bit resolution for coding analogue signals. This results in 256 bins in the probability distribution. It is possible that in the future the video signal will be coded with greater accuracy using perhaps up to ten bits. The analyser has therefore been designed with a 1024 bin store to ensure compatibility in the future.

(D) What is the vertical resolution of the display?

As a result of conditions B and C the PDF is stored in 1024 bins, each value being represented by a 16 bit word. This must be converted into a suitable analogue signal which can be displayed on an oscilloscope. The stored distribution has a potential dynamic range of 65,536 different levels but the vertical resolution of an oscilloscope is insufficient to display this range. A sensible solution is to restrict the amplitude of the displayed PDF to 8 bits corresponding to 256 different vertical positions on an oscilloscope display. An adjustable window is then required so that the user can select a slice of 8 bits of the stored PDF depending on the dynamic range of the signal.

4. Description of the analyser

4.1. Introduction

The design of the analyser is based on two stores, one, a fast store for data acquisition and the

other, a slow store for display. A new PDF is built up during the active field while the old one is being displayed. At the end of the active field the new PDF is transferred from the fast to the slow store ready for display during the subsequent field. The circuit is thus divided into acquisition, display and housekeeping blocks.

4.2. Acquisition circuit

The basic idea of the PDF accumulator is shown in Fig. 1. Each incoming data value corresponds to a particular location in a 1024 × 16 bit RAM and the contents of each location represent the number of times that that particular value has occurred in the current measurement period. As each incoming data value occurs it addresses the RAM and the contents of the appropriate location are read, incremented by one, and written back into the same location. In this way the PDF is accumulated until the process is stopped at the end of the measurement period. The accumulated PDF is then transferred to the display store and, at the same time, the acquisition store is cleared, ready for the next measurement period.

Unfortunately the memory cycles of easily available store devices are not fast enough to enable the read, increment and write operations to be carried out in one sampling interval at the fastest data rates. So it is necessary to demultiplex the data three ways to obtain a reasonable working speed and triplicate the circuit of Fig. 1, each circuit working in one phase of a 3-phase cycle. The PDFs accumulated in each store are then added together during the transfer process at the end of the measurement period.

The measurement period corresponds, nominally, to the active field period but, depending on the application, it may be desirable to suppress measurement during the line blanking intervals. This can be done simply by suspending the data input to the accumulator circuits during line blanking by inhibiting the operation of 3 latches on the input. Care must be taken, however, to ensure that each of the 3 circuits completes its memory cycle at the end of the complete measurement period.

In addition, it is sometimes convenient to be able to freeze the PDF obtained during any particular field. This can be done simply by inhibiting the active field signal. This will cause the PDF to be acquired and transferred once only and then repeatedly displayed.

4.3. Display circuit

The display requires the contents of the store to be scanned repeatedly and, in principle, this could be done using the acquisition store if it were fast enough to allow sequential reading interleaved with random updating during the measurement period. However, as this is not so, a separate store is needed.

The speed of the second store is governed by the store-to-store transfer time, which must be less than the field blanking interval, and the required repetition rate of the display. A repetition period of nominally 1 ms was chosen as being of the same order as the transfer time. This is low enough to give a reasonable number of scans per PDF (so that end-effects of fractional scans can be neglec-

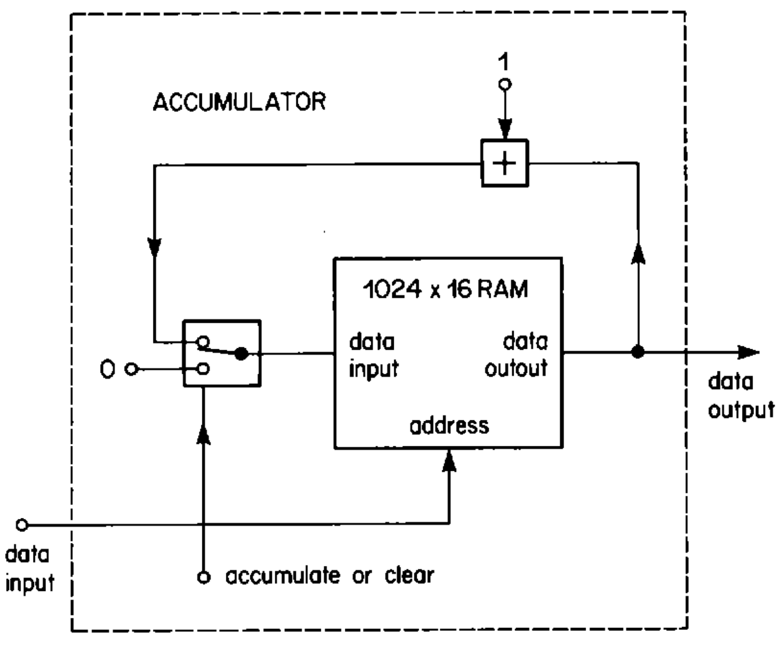

Fig. 1—The basic accumulator circuit.

ted). As the store contains 1024 locations the 1 kHz repetition rate implies a reading clock rate of about 1 MHz, which is still low enough to enable a comparatively low-speed digital-to-analogue converter to be used.

The output of the DAC is, ideally, a "boxcar" or histogram display of the store contents, assuming the following amplifier has enough bandwidth to respond adequately to the discontinuities. However, in practice, the output must be lowpass filtered to remove glitches and breakthrough of the high-speed clocks associated with the acquisition circuit. A filter cut-off frequency of 1 MHz was chosen as a compromise between noise suppression and reasonable preservation of the boxcar form.

The display store is partitioned into 4 blocks which can be separately scanned. This is useful where two of the input data bits are used to qualify the other 8. The scanned block can be selected by a 4-position manual control. In this case the repetition rate of the display is increased fourfold.

As mentioned in Section 3, the full 16-bit resolution of the store is not needed for display. Thus the store output is passed through a bit-shifter which selects an 8-bit slice of the data before it is passed on to the DAC. The position of the slice can be varied by an 8-position manual control. The "slicer" contains no limiter so that if bits above the significance level of the slice change, a characteristic modulo-8 behaviour will result.

4.4. Miscellaneous circuit details

A block diagram of the complete analyser is shown in Fig. 2. The circuit is divided into 3 blocks as mentioned above. Demultiplexing of the input data is performed by three synchronous counters which also function as latches that can be enabled via their LOAD inputs. The enabling waveforms are derived from a 3-phase circuit and ensure that the latches capture interleaving data values. The 3 phase circuit is enabled by the MEASURE/$\overline{\text{COPY}}$ signal and also by the MEASUREMENT ENABLE signal which corresponds nominally to the active line period.

At the end of the measurement period data is transferred from the accumulators by switching the latch/counters to their counting mode via the ENABLE COUNT inputs and disabling the LOAD inputs. The ENABLE COUNT waveform is derived from the system clock and causes the counter to increment once every 8 system clocks, thereby effectively counting at $\frac{1}{8}$ of the system clock rate. At the same time the display store counter is also caused to count at the same rate by similar means except that the phase of the count must be delayed to allow for the processing time of the 3-way adder. The total time for data transfer is thus 8192 system clock periods which, for an input data frequency of 851 $\times$ line frequency f_L, is 616 μs.

The system then remains in an idle state until the beginning of the next measurement period. The length of the idle time is about 1 ms before measurement and display begin again. During display, the ENABLE COUNT waveform generator for the display counter is switched to divide the system clock by 14 and thus cause the display counter to count at $\frac{1}{14}$ of the system clock rate. The repetition period of the display is thus 14336 system clock periods which, for 851 f_L data, is 1.078 ms. This is reduced 4-fold for quadrant display.

The "8-bit window" function is performed by parallel-serial converters which load the incoming data and then shift it a given number of places, one place per system clock period, according to the number of clock pulses received from a counter. As the data rate is $\frac{1}{14}$ of the system clock it is thus possible, in principle, to shift by up to 14 places. Varying the shift does, of course, vary the phase of the data which enter the DAC but this effect is of no significance. The DAC is simply a precision current weighting circuit and does not require clocks. Noise and glitches are removed by post-filtering as previously noted.

The housekeeping circuit produces all the waveforms necessary to drive the counters and stores together with the system clock. The phasing of these waveforms is determined by the input horizontal and vertical WINDOW waveforms. These waveforms would normally be available from the data source and correspond, nominally, to the active line and field periods. Fig. 3 is a timing diagram showing the phasing of the analyser states relative to the vertical window waveform.

5. Experimental applications

Two experimental applications will be described which illustrate how the analyser may be used. Each application will be considered in turn; a brief description of the theoretical basis for the distributions is given, together with photographs of measured distributions.

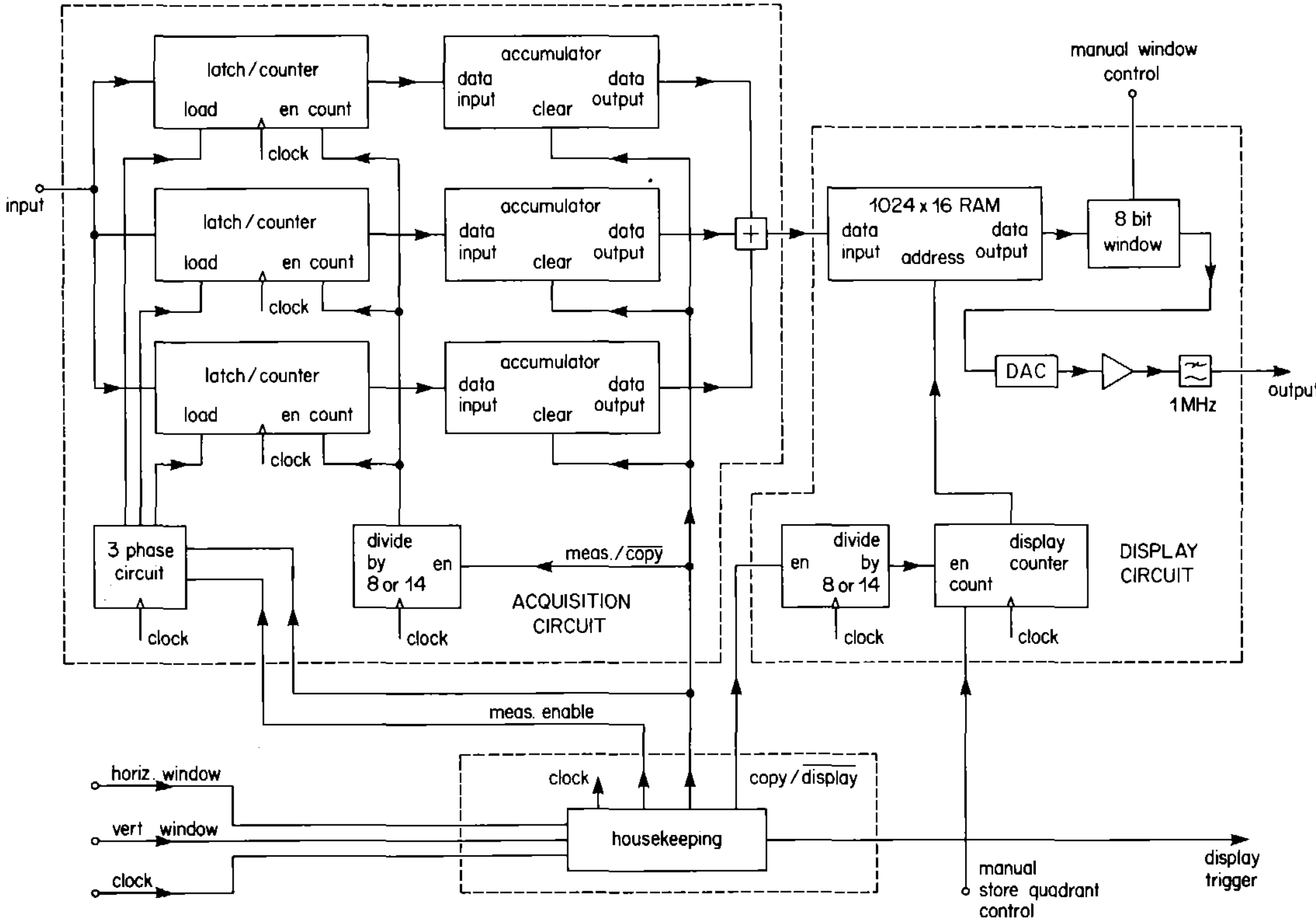

Fig. 2—Block diagram of the analyser.

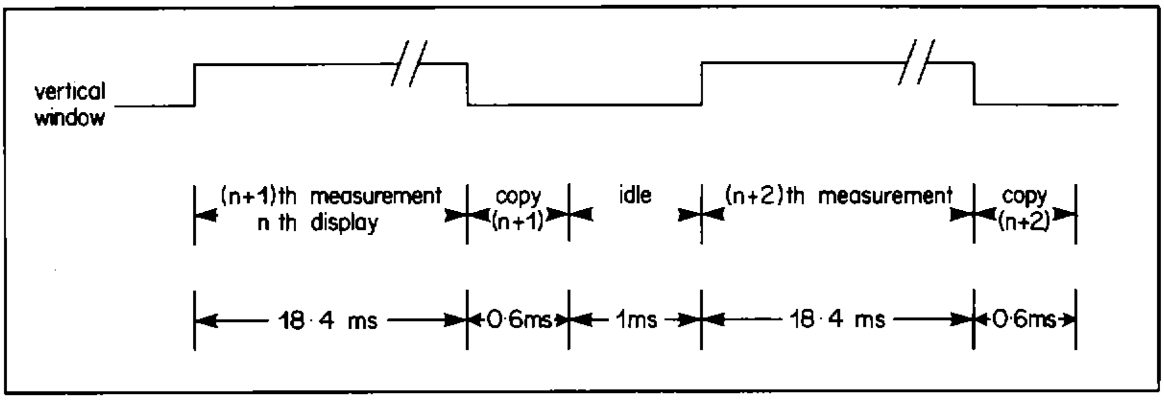

Fig. 3—Relative timing between analyser states and vertical window waveform.

5.1. Differential pulse code modulation (DPCM)

DPCM coding is a method for reducing the number of bits/sample required to represent a picture signal. It exploits the statistical properties of picture information and also the limitations of visual perception. An important element of a DPCM coder is a predictor circuit which can accurately predict any picture sample from a weighted combination of previously decoded sample values. In a DPCM system a prediction-error signal, equal to the difference between the predicted and actual sample value, is formed and this is non-linearly quantised for transmission. At the receiver an inverse procedure is employed to reconstruct the signal. Ideally the predictor output should be equal to the actual sample value. In practice, the perfect predictor cannot be made and the difference signal is not identically zero but depends on the data. The PDF of the difference signal is a useful measure of the predictor performance. If the PDF is sharply peaked around zero with a limited spread of the skirts of the distribution it will be possible to concentrate the decision levels of the quantiser near the origin. This will minimise the picture impairment for a given number of bits/sample. The experimental arrangement for measuring the PDF is shown in Fig. 4.

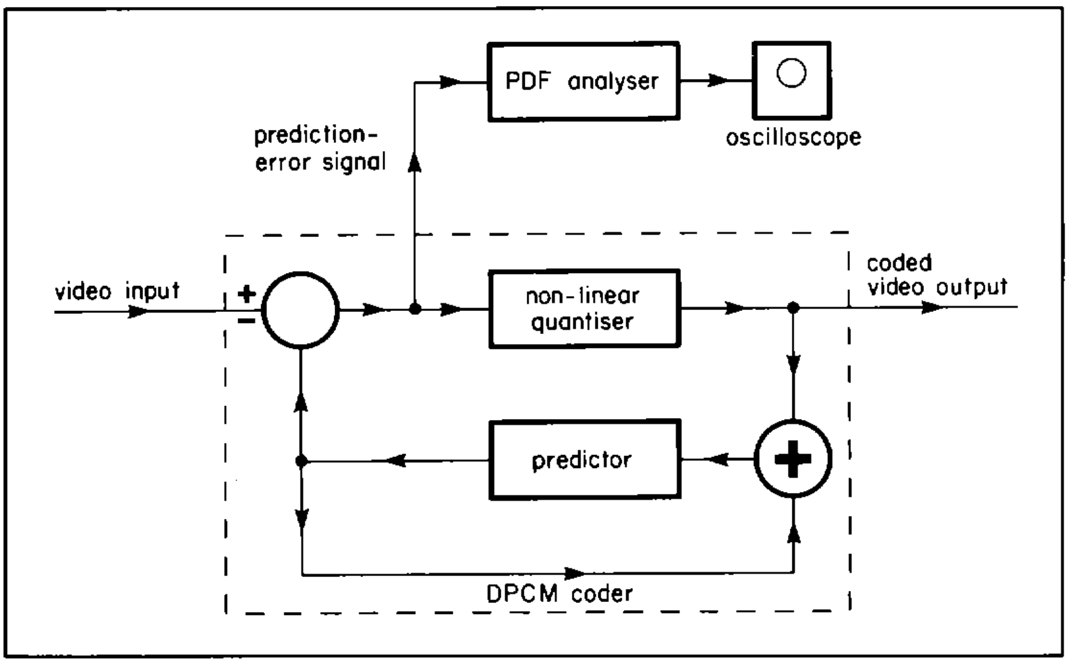

Fig. 4—Experimental arrangement for measuring the PDF of the prediction-error signal in a DPCM coder.

Figure 5 shows a PDF of the prediction-error signal using a three dimensional predictor [1] whose coefficients have previously been determined by a computer optimisation. The PDF† is sharply peaked and indicates that the coefficients are well chosen. On the other hand Fig. 6 shows the PDF† of a less than optimum predictor. In this case the skirts of the distribution are more widely spread illustrating that a poor predictor has been used.

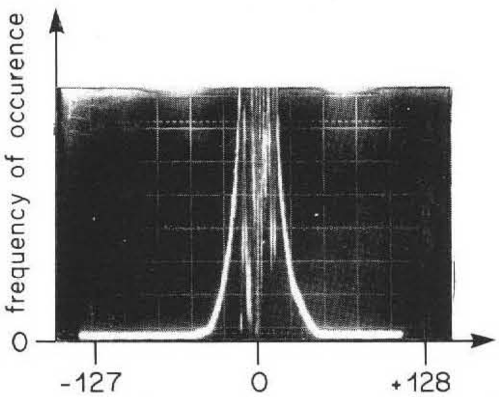

Fig. 5—PDF of the prediction-error signal for an optimised predictor.

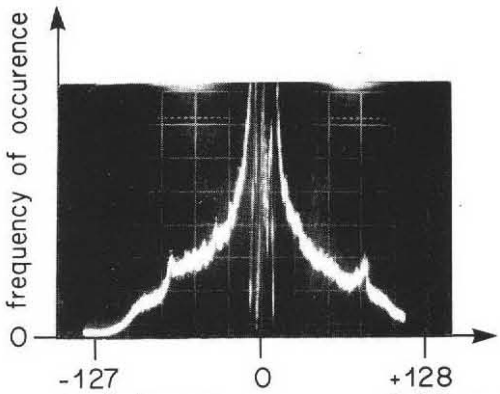

Fig. 6—PDF of the prediction-error signal for an unoptimised predictor.

5.2. Noise reduction

The BBC Research Department video noise reducer (2)‡ has a movement detection circuit which uses a processed picture-difference signal. This signal contains two components, one a variable component due to motion and the other a quiescent component due to noise. To detect motion correctly, therefore, the quiescent value must be known. This is done using a noise measurement circuit. In a stationary picture the PDF of the processed picture difference signal only contains information about the noise. In fact the mode of the distribution is proportional to the noise voltage. However, when movement occurs the distribution is modified and additional peaks may be introduced.

The analyser has been used to display the dynamically changing PDF. Observing how the movement contribution rides on top of the noise signal may suggest new ways of separating the noise component from the movement. Two measurements were made using the experimental arrangement shown in Fig. 7. A source of "off air" pictures was monitored and the PDF photographed during a momentarily stationary scene. A short while later movement in the same scene occurred and a second photograph was taken. Figures 8 and 9 show the photographs. For the stationary scene the associated PDF has a single peak whose position on the x-axis is a function of the noise power in the input picture. The second photograph shows an additional peak which has been introduced by the movement.

6. Future developments

The analyser has proved itself to be a very powerful tool in both the DPCM and video noise reduction investigations. It does however have an important limitation in that the PDF can only be observed qualitatively on an oscilloscope. The analyser would be even more useful if it contained a two dimensional cursor. This could be used, for example, to measure the positions and amplitudes of maximum and minimum points in the distribution.

More complex processing could be achieved by including an interface in the analyser which allowed a computer to access the stored PDF. Programs could then be written to measure those features in the distribution which were of particular interest.

† The display window has been adjusted to magnify the dynamic range of the outer bins in the distribution. This however causes the central bins to overflow and is the cause of the streaky detail in the central region.

‡A production design of this equipment is manufactured by Pye TVT Limited.

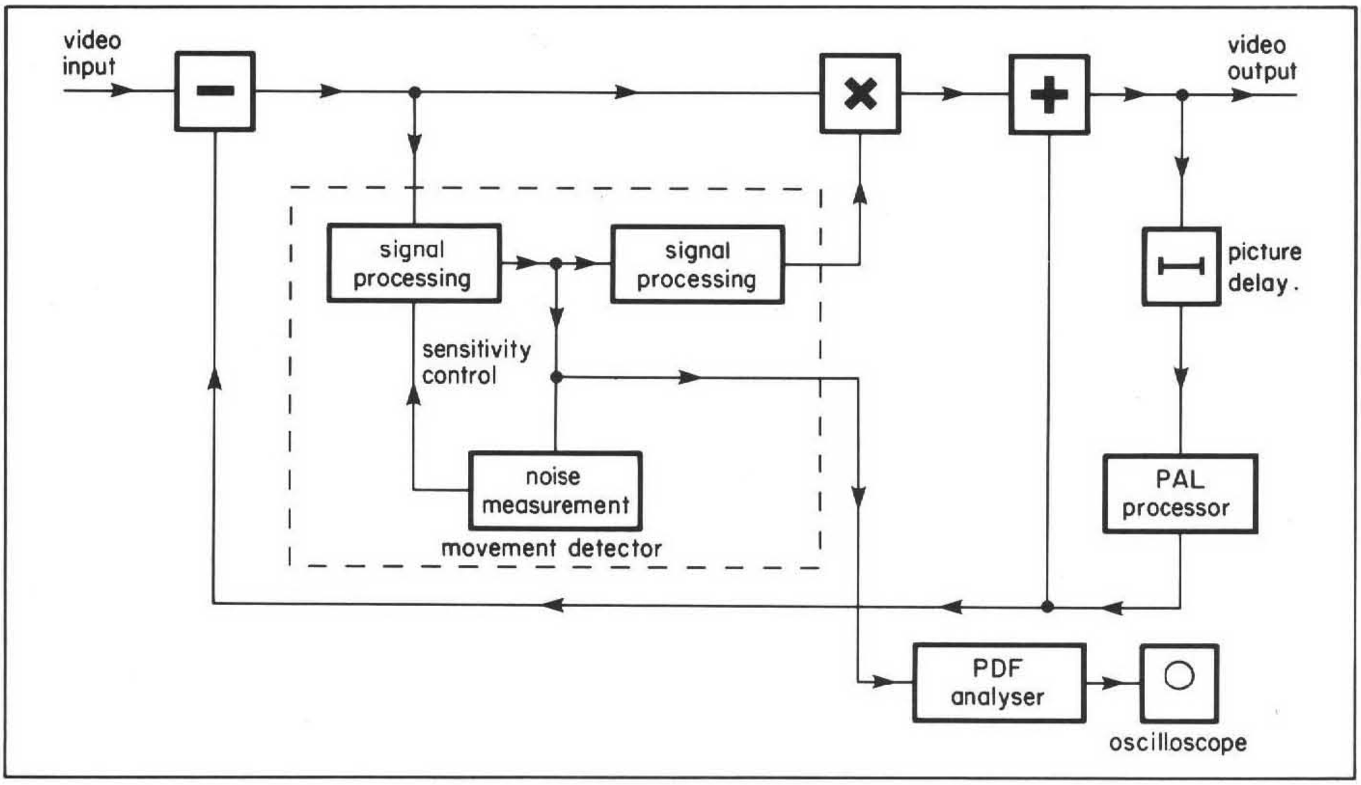

Fig. 7—Experimental arrangement for measuring the PDF of the processed picture-difference signal in a video noise reducer.

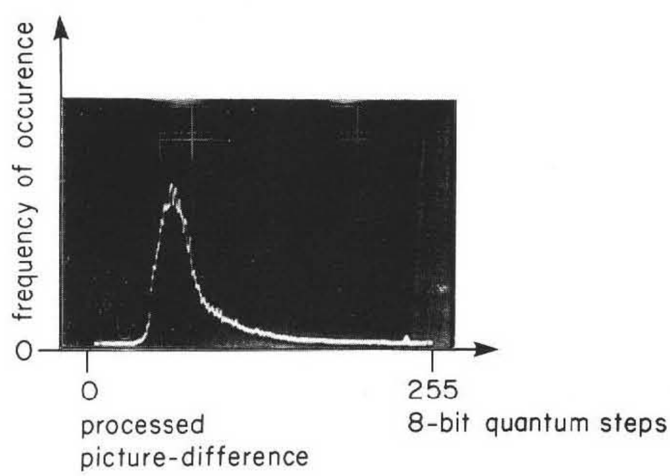

Fig. 8—PDF of the processed picture-difference signal in a noise reducer during a momentarily stationary scene.

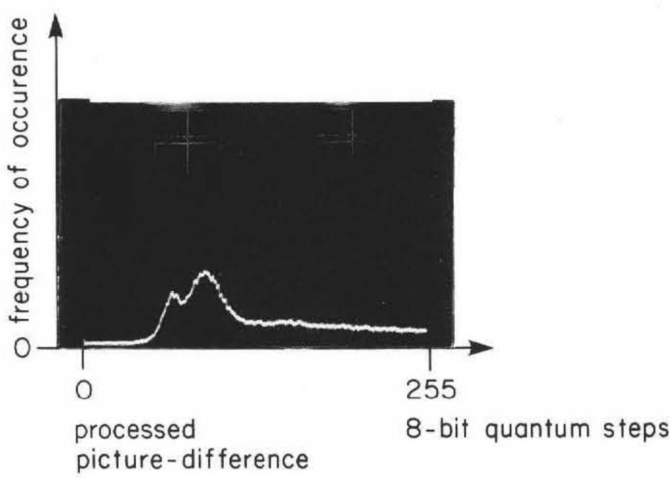

Fig. 9—PDF of the processed picture-difference signal in a noise reducer during movement in the same scene as Fig. 8.

7. Conclusion

An analyser has been successfully developed to measure the probability distribution function of digital video signals. Previously these measurements could not have been performed since suitable means were not available. It is hoped that data obtained from the analyser will provide an insight into developing improved algorithms for processing digital video signals.

8. References

1. RATLIFF, P. A., 1978. "Bit-rate reduction for high quality digital television transmission". IBC 78, IEE Conf. Pub. 166, pp. 37–41.

2. DREWERY, J. O., "An Adaptive Video Noise Reducer". BBC Research Department Report in preparation.

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